and a comparator stage 1407 that generates output signals (e.g., the Upper_Threshold Signal and Lower_Threshold Signal) that indicate the time period when the positive and negative peaks of the amplified first derivative signal produced by the amplifier stage exceed predetermined thresholds (i.e., a positive peak level PPL and a negative peak level NPL).

On Page 69, amend the last paragraph as follows:

The signal conditioning circuitry 903 operates to smooth out or otherwise filter the scan data signal produced by the photodetector 902 to remove unwanted noise components therein, and possibly amplify such signal. An illustrative implementation of such signal conditioning circuitry is described below with respect to ~~Fig. 11~~ Figs. 11A and 11B. The output of the signal conditioning circuitry 903 is provided to the plurality of signal processing paths (two shown as path A and path B) that process the output of the signal conditioning circuitry 903 in parallel.

On Page 70, amend the last paragraph as follows:

The first derivative threshold circuitry in each respective path (labeled 905-A and 905-B) operates as a positive and negative peak detector to provide output signals that indicate the approximate time periods when the positive and negative peaks of the first derivative signal provided thereto exceed predetermined thresholds (i.e., a positive peak level PPL and a negative peak level NPL). An illustrative implementation of such first derivative threshold circuitry 905 for the two different paths is described below with respect to ~~Fig. 14~~ Figs. 14A through 14C.

On Page 73, amend the last paragraph as follows:

~~Fig. 11~~ Figs. 11A and 11B, taken together, illustrates an exemplary embodiment of the signal conditioning circuitry 903 of Fig. 9, which operates to amplify and smooth out or otherwise filter the scan data signal produced by the photodetector 902 to remove unwanted noise components therein. The circuitry 903 comprises, a number of subcomponents arranged in a serial manner, namely: a high gain amplifier stage 1103, a multistage amplifier stage 1105, a differential amplifier stage 1107 and a low pass filter (LPF) stage 1109. The amplifier stages 1103, 1105 and 1109 amplify the voltage of the analog scan data signal produced by the photodetector 902 with gains of 90, 3.0 and 7.1, respectively, to provide a total gain of about 1900. The low pass filter 1109 stage operates to filter out unwanted noise in the amplified signal

produced by the amplifier stages 1103, 1105 and 1109. The 3dB cutoff frequency of the low pass filter shown (which is a maximally flat Butterworth type filter) is approximately 780 kHz, which is designed to filter out unwanted high frequency noise (e.g., noise which lies above the expected maximum signal frequency of 540 kHz).

On Page 78, amend the last paragraph as follows:

~~Fig. 14~~ Figs. 14A through 14C illustrate exemplary implementation of the first derivative signal threshold circuitry 905, which is suitable for use in the two different paths of the scan data signal processor of Fig. 9. As shown in ~~Fig. 14~~ Figs. 14A through 14C, the first derivative signal threshold circuitry 905 includes an amplifier stage 1401 that amplifies the voltage levels of the first derivative signal produced by the first derivative signal generation circuitry 904, positive and negative peak detectors 1403 and 1405, and a comparator stage 1407 that generates output signals (e.g., the Upper_Threshold Signal and Lower_Threshold Signal) that indicate the time period when the positive and negative peaks of the amplified first derivative signal produced by the amplifier stage exceed predetermined thresholds (i.e., a positive peak level PPL and a negative peak level NPL). Preferably, the positive peak level PPL and negative peak level NPL are dynamic thresholds (e.g., these levels change as the amplified analog signal changes over time) based upon a DC bias level and a percentage (portion) of the amplified first derivative signal produced by the amplifier stage 1401. In the illustrative embodiment shown in ~~Fig. 14~~ Figs. 14A through 14C, capacitors C16 and C18 are configured as peak detectors (with a decay time constant proportional to the values of R14/C16 and R19/C18, respectively); and the positive peak level PPL is set by the resistance values of the resistor network R16,R17,R18 and R_{U_BIAS}, while the negative peak level NPL is set by the values of the resistor network R21,R22,R23 and R_{L_BIAS}.